

## CLAIMS

What is claimed is.

*Sub B12*

1. A method of forming a device comprising:  
patterning a first oxide upon a substrate;  
forming a first nitride spacer mask upon the first oxide;  
forming a first oxide spacer mask upon the first nitride spacer mask;  
forming a second nitride spacer mask upon the first oxide spacer mask;  
forming a plurality of channels in the substrate that are aligned to the second

7 nitride spacer mask; and

8 forming a gate layer over the plurality of channels, wherein each of the plurality  
9 of channels is narrower than the mean free path of semiconductive electron flow therein.

1 2. The method according to claim 1, wherein forming a first nitride spacer mask  
comprises:

3 forming a first nitride layer over the first oxide; and  
4 performing a reactive ion etch upon the first nitride layer.

1 3. The method according to claim 1, wherein forming a first oxide spacer mask upon  
the first nitride spacer mask comprises:

3 forming a first oxide layer over the first nitride spacer mask; and  
4 performing a reactive ion etch upon the first oxide layer.

1           4. The method according to claim 1, wherein forming a second nitride spacer mask  
2 upon the first oxide spacer mask comprises:

3                 forming a second nitride layer over the first oxide spacer mask; and  
4                 performing a reactive ion etch upon the second nitride layer.

1           5. The method according to claim 1, wherein forming a plurality of channels in the  
2 substrate that are aligned to the second nitride spacer mask comprises:  
3                 performing a gate etch with the second nitride spacer masks.

1           6. The method according to claim 1, wherein forming a first nitride spacer mask  
2 comprises:

3                 forming a first nitride layer over the first oxide; and  
4                 performing a reactive ion etch upon the first nitride layer, wherein forming a first  
5 oxide spacer mask upon the first nitride spacer mask comprises:

6                 forming a first oxide layer over the first nitride spacer mask; and  
7                 performing a reactive ion etch upon the first oxide layer, wherein forming a  
8 second nitride spacer mask upon the first oxide spacer mask comprises:

9                 forming a second nitride layer over the first oxide spacer mask; and  
10                 performing a reactive ion etch upon the second nitride layer, wherein forming a  
11 plurality of channels in the substrate that are aligned to the second nitride spacer mask  
12 comprises:

13                 performing a gate etch with the second nitride spacer masks, and further  
14 comprising: forming a gate oxide upon the plurality of channels.

1           7.     The method according to claim 1, wherein the first oxide is patterned with a width

2     of about 100 nm and a pitch of about 300 nm.

1           8.     The method according to claim 1, wherein the first oxide is patterned with a width

2     of about 100 nm and a pitch of about 320 nm.

1           9.     The method according to claim 1, wherein the substrate is made by providing a

2     silicon on insulator substrate, and wherein the plurality of channels comprises monocrystalline

3     silicon channels.

1           10.    The method according to claim 1, wherein the substrate comprises

2     monocrystalline silicon, and wherein the plurality of channels is spaced apart by a trench that is

3     at least as wide as each of the channels.

1           11.    The method according to claim 1, wherein the substrate comprises

2     monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at

3     least as wide as each of the channels, and wherein a doping region is disposed in the substrate

4     beneath the trench that resists electrical communication between adjacent spaced-apart channels.

1           12.    The method according to claim 1, wherein the substrate comprises

2     monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at

3     least as wide as each of the channels, wherein the trench is filled with a dielectric, and wherein

4 the plurality of channels comprises a plurality of single-gate quantum wire field effect  
5 transistors.

1 13. The method according to claim 1, wherein the substrate comprises  
2 monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at  
3 least as wide as each of the channels, wherein each of the plurality of channels has a gate oxide  
4 layer disposed thereupon, and wherein the second nitride spacer mask is disposed between the  
5 channel and the gate layer.

1 14. The method according to claim 1, wherein the plurality of channels comprises a  
2 plurality of triple-gate quantum wire field effect transistors.

1 15. The method according to claim 1, wherein the substrate comprises  
2 monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at  
3 least as wide as each of the channels, wherein a doping region is disposed in the substrate  
4 beneath the trench that resists electrical communication between adjacent spaced-apart channels,  
5 and wherein the substrate is part of a silicon on insulator structure.

1 16 A method of forming a device comprising:  
2 patterning a first oxide having a first width upon a substrate;  
3 forming a first nitride layer upon the first oxide and the substrate, wherein the first  
4 nitride layer has a first thickness that is less than the first width;  
5 forming a first nitride spacer mask from the first nitride layer, wherein the first  
6 nitride spacer mask has a width equal to the first nitride layer thickness;  
7 forming an oxide layer upon the first nitride spacer mask, wherein the oxide layer  
8 has a second thickness that is less than the width of the first nitride spacer mask;  
9 forming a first oxide spacer mask from the oxide layer, wherein the first oxide  
10 spacer mask has a width equal to the first oxide layer thickness;  
11 forming a second nitride layer upon the first oxide spacer mask, wherein the  
12 second nitride layer has a thickness that is less than the width of the first oxide spacer mask;  
13 forming a second nitride spacer mask from the second nitride layer;  
14 removing the first oxide spacer mask;  
15 performing an etch over the second nitride spacer mask to form at least one  
16 semiconductor channel having a channel width and a length, wherein the mean free electron path  
17 therein is larger than the channel width;  
18 forming a dielectric layer upon the channel length; and  
19 forming a gate layer over the channel.

1 17. The method according to claim 16, wherein the first oxide has a width of X and a  
2 pitch of about 3X.

1        18. The method according to claim 16, wherein each performing a spacer etch  
2        comprises performing a reactive ion etch.

1        19. The method according to claim 16, further comprising:  
2        performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3        topology of a plurality of semiconductor channels, wherein each of the plurality of  
4        semiconductive channels has a width of about one-tenth X;  
5        forming an oxide upon the SOI topology; and  
6        forming a gate layer over the oxide.

1        20. The method according to claim 16, further comprising:  
2        performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3        topology of a plurality of semiconductor channels wherein the mean free electron path in each of  
4        the plurality of channels is larger than about one-tenth X;  
5        removing the patterned second nitride spacer mask;  
6        forming an oxide upon the SOI topology; and  
7        forming a gate layer over the oxide.

1        21. The method according to claim 16, further comprising:  
2        performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3        topology of a plurality of semiconductor channels wherein the mean free electron path in each of  
4        the plurality of channels is larger than about one-tenth X;  
5        forming an oxide upon the SOI topology;

6 forming a gate layer over the oxide; and

7 forming a contact that connects with the plurality of channels, wherein the contact has a

8 characteristic width from about 2X to about 10X.

1 22. A method of forming a device comprising:  
2 patterning a first oxide upon a substrate, wherein the first oxide has a  
3 characteristic width of  $X$  and a characteristic pitch selected from about  $3X$  and about  $3.2X$ :  
4 forming a first nitride layer upon the oxide, wherein the first nitride layer has a  
5 characteristic thickness of about one half  $X$ ;  
6 performing a spacer etch upon the nitride layer and removing the oxide to form a  
7 patterned first nitride spacer mask;  
8 forming an oxide layer upon the patterned first nitride spacer mask, wherein the  
9 oxide layer has a characteristic thickness of about one fourth  $X$ ;  
10 performing a spacer etch upon the oxide layer and removing the patterned first  
11 nitride spacer mask to form a patterned first oxide spacer mask;  
12 forming a second nitride layer upon the patterned first oxide spacer mask, wherein  
13 the second nitride layer has a characteristic thickness of about one-tenth  $X$ ; and  
14 performing a spacer etch upon the second nitride layer and removing the first  
15 oxide spacer mask to form a patterned second nitride spacer mask.

1 23. The method according to claim 22, further comprising:  
2 performing an etch over the patterned second nitride spacer mask to form at least  
3 one semiconductor channel wherein the mean free electron path therein is larger than about one-  
4 tenth  $X$ .

1 24. The method according to claim 22, wherein  $X$  is in a range from about 20 nm to  
2 about 200 nm.

1        25. The method according to claim 22, wherein each performing a spacer etch  
2        comprises performing an reactive ion etch.

1        26. The method according to claim 22, further comprising:  
2            performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3            topology of a plurality of semiconductor channels wherein the mean free electron path in each of  
4            the plurality of channels is larger than about one-tenth X;  
5            forming an oxide upon the SOI topology; and  
6            forming a gate layer over the oxide.

1        27. The method according to claim 22, further comprising:  
2            performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3            topology of a plurality of semiconductor channels wherein the mean free electron path in each of  
4            the plurality of channels is larger than about one-tenth X;  
5            removing the patterned second nitride spacer mask;  
6            forming an oxide upon the SOI topology; and  
7            forming a gate layer over the oxide.

1        28. The method according to claim 22, further comprising:  
2            performing an etch over the patterned second nitride that forms a silicon on oxide (SOI)  
3            topology of a plurality of semiconductor channels wherein the mean free electron path in each of  
4            the plurality of channels is larger than about one-tenth X;  
5            forming an oxide upon the SOI topology;

6 forming a gate layer over the oxide; and

7 forming a contact that connects with the plurality of channels, wherein the contact has a

8 characteristic width from about 2X to about 10X.

1 29. A device comprising:  
2 a plurality of semiconductive channels, each of the plurality of semiconductive  
3 channels comprising a channel length and a channel width;  
4 a dielectric layer disposed upon the semiconductive channel length;  
5 a source at a first terminal end of the plurality of semiconductive channels, and a  
6 second terminal end of the plurality of semiconductive channels;  
7 a gate layer disposed over the dielectric layer, wherein electron flow in the  
8 plurality of semiconductive channels has a mean free path that is greater than the  
9 semiconductive channel width, and wherein a first semiconductive channel is spaced  
10 apart from a second semiconductive channel by a trench that is less than about five times  
11 the semiconductive channel width.

1 30. The device according to claim 29, wherein the plurality of semiconductive  
2 channels comprises monocrystalline silicon that is disposed upon a dielectric.

1 31. The device according to claim 29, wherein the plurality of semiconductive  
2 channels comprises monocrystalline silicon that has a self-aligned doping region in the  
3 monocrystalline silicon beneath the trench.

1 32. The device according to claim 29, further comprising:  
2 a mask disposed upon the semiconductive channel width, wherein the device  
3 comprises a double-gate quantum wire.

1       33. The device according to claim 29, wherein the semiconductive channel width is in  
2                   a range from less than or equal to about 5 nm to about 30 nm.

1       34. The device according to claim 29, further comprising:  
2                   a mask disposed upon the semiconductive channel width, wherein the trench is  
3                   filled with material comprising the gate layer.

1       35. The device according to claim 29, wherein the device comprises a triple-gate  
2                   quantum wire.

1       36. The device according to claim 29, further comprising:  
2                   a contact that makes electrical connection with one of the terminal ends of the  
3                   plurality of semiconductive channels upon a contact landing pad.

1       37. The device according to claim 29, further comprising:  
2                   a contact that makes electrical connection with one of the terminal ends of the  
3                   plurality of semiconductive channels, wherein the contact has a characteristic width in a  
4                   range from about 200 nm to about 1,000 nm.

1       38. The device according to claim 29, further comprising:  
2                   a trench disposed between the first semiconductive channel and the spaced-apart  
3                   second semiconductive channel, wherein the trench is filled with the dielectric material that is  
4                   disposed on the semiconductive channel length.

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